

**EXHIBIT “A”**

UNITED STATES DISTRICT COURT  
EASTERN DISTRICT OF PENNSYLVANIA

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JERALD BATOFF,

Plaintiff,

Civil Action

v.

JULIE CHARBONNEAU and  
DEAN TOPOLINSKI

Defendants.  
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**AFFIDAVIT OF SHUKRI SOURI, Ph.D.**

Shukri Sourì, being sworn, deposes and says:

A. Background and Qualifications

1. I hold a Ph.D. degree in Electrical Engineering from Stanford University.
2. I am a Principal, Practice Director and Office Director of the Electrical Engineering & Computer Science practice of Exponent Failure Analysis Associates in New York. My qualifications are as set forth in my curriculum vitae and are set forth in more detail in defendants' motion to exclude experts. (Exhibit A).
3. In preparing the opinions expressed in this affidavit, among other things, I have participated in an inspection at 200 South Ithan Avenue, Villanova, Pennsylvania, including, but not limited to, inspecting the residence, wiring, and circuit breakers. I also inspected and tested, the circuit breaker panel and sub-panel including breaker 25.

4. During the inspection of the residence at 200 South Ithan, I observed wiring in the basement that had noticeable arcing with a separation of approximately an inch between the two ends of the arced wires ("Arced Wires").

5. I traced the Arced Wires to the breaker panel and determined that they were connected to breaker 25. Breaker 25 did not trip during the fire and remained, at the time of my inspection, in the operating position.

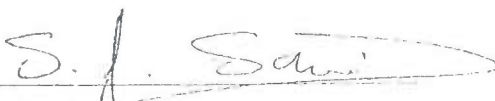
6. Subsequently, I inspected and tested the circuit breaker panel, sub-panel and breaker 25. My inspection and testing revealed that all were operating appropriately.

7. In my opinion, if an electrical event caused the Arced Wires to be in the condition that I observed, breaker 25 should have tripped.

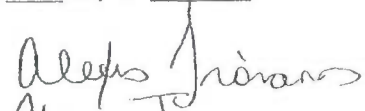
8. In my opinion, and based on the above, no natural event could have caused the Arced Wires to be in the condition I observed during my inspection.

9. In my opinion, an intentional external non-electrical force caused the wires to arc, separate by approximately an inch and caused the wires to be in the condition that I observed.

10. All of the opinions expressed herein are within a reasonable degree of scientific and engineering certainty.

  
Shukri J. Sour

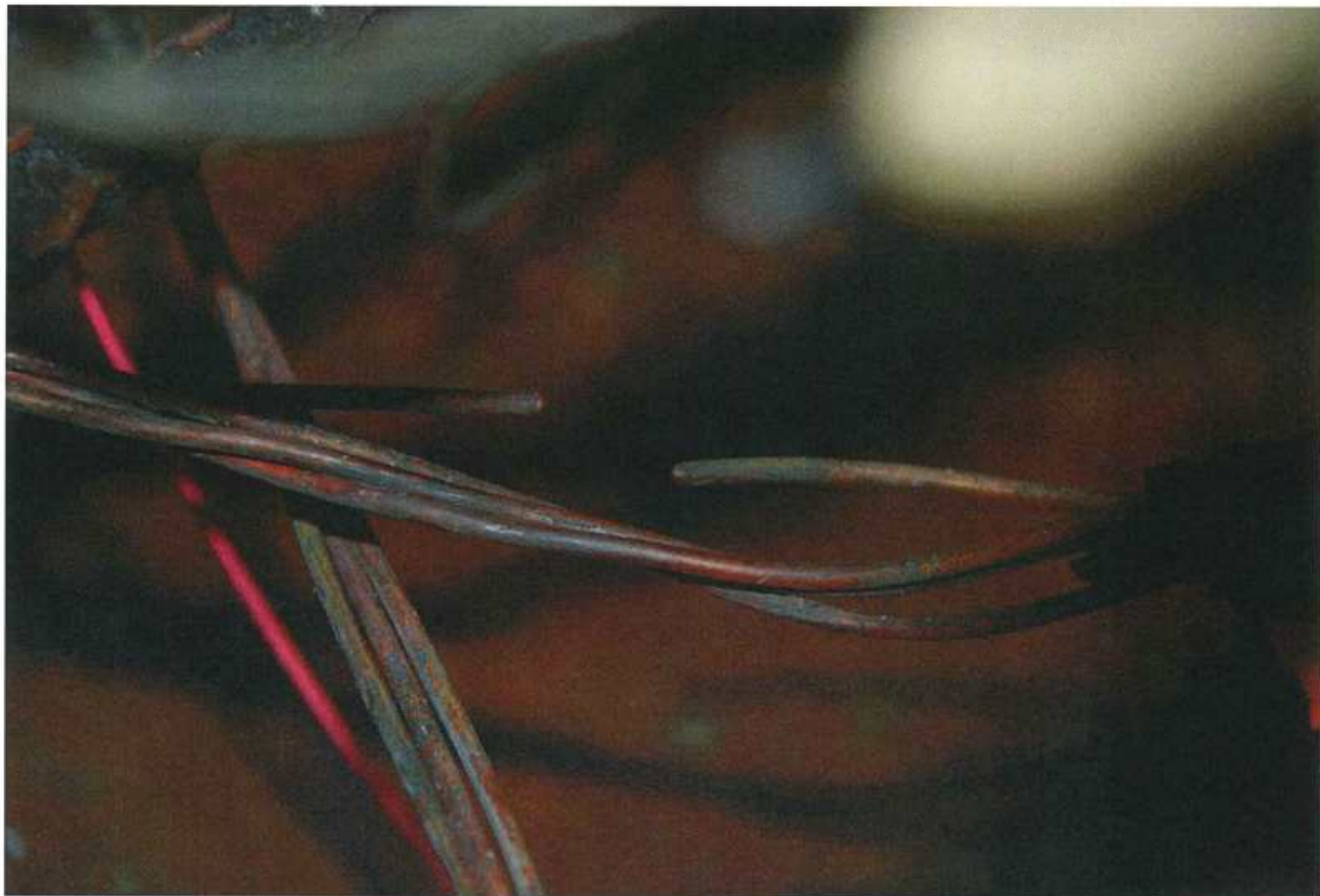
Sworn to before me this  
22 day of October, 2012.

  
Alexis Troianos

Notary Public

ALEXIS TROIANOS  
NOTARY PUBLIC-STATE OF NEW YORK  
No. 01TR6268166  
Qualified in New York County  
My Commission Expires August 27, 2016







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**Shukri J. Sourì, Ph.D.**  
**Principal, Practice Director and Office Director, New York**

**Professional Profile**

Dr. Shukri Sourì is a Principal and Director of Exponent's Electrical Engineering and Computer Science practice and is the Director of Exponent's New York office. Dr. Sourì's background is in electrical and electronic engineering and computer systems. His professional activities include addressing issues related to electrical components, semiconductors, integrated circuits (ICs), electronics and software. His specialties include intellectual property analysis, manufacturing, reliability and failure analysis of electronic products and assemblies, medical devices, optical systems, computer memories, circuit protection, automotive electronics, computer communications, networks, and software.

Dr. Sourì received his Ph.D. in Electrical Engineering at Stanford University on 3-Dimensional integration of ICs and has taught several courses on IC fabrication, optical fiber communications, TCP/IP networking, and communications protocols and implementation of systems on 3-D chips. He also read Engineering Science at Balliol College, Oxford, where he specialized in photorefectance microscopy of semiconductor materials. His research interests include: solid state light emitting devices; semiconductor materials, devices and fabrication processes; microprocessor architecture and circuit design; audio/video/image processing software and content delivery technologies; medical devices including resectoscopes, cochlear implants and ICDs; embedded controls systems for computer hard disk drives; IC packaging and printed circuit board assembly; display technologies; telephony, mobile communications, and networking.

**Academic Credentials and Professional Honors**

Ph.D., Electrical Engineering, Stanford University, 2003  
M.S., Electrical Engineering, Stanford University, 1994  
M.A., Oxford University (U.K.), 2007  
B.A. (Honors), Engineering Science, Oxford University (U.K.), 1992

## **Patents**

Patent 6,188,556: Two-Terminal Transistor PTC Circuit Protection Devices, WO0024126, 2001 (with C. McCoy, H. Duffy, A. Cogan, and R. Bommakant).

Patent 6,181,541: Transistor-PTC Circuit Protection Devices, WO0024105, 2001 (with H. Duffy, A. Cogan, M. Munch, and N. Nickols).

Patent 6,153,948: Electronic Circuits with Wide Dynamic Range of On/Off Delay Time, WO001249, 2000 (with A. Cogan).

Patent 5,569,495: Method of Making Varistor Chip with Etching to Remove Damaged Surfaces, CA2220931, EP0826225, WO963978, JP11505375T, 1996 (with A. Evans, T. Tsukada, and R. Dupon).

## **Publications**

D'Andrade B, Kattamis AZ, Murphy PF, McNulty J, Souri S. Arcing enabled by tin whiskers. IEEE: Reliability Society 2010 Annual Technical Report, 2010.

Fu J, Souri S, Harris J. Temperature and humidity dependent reliability analysis of RGB LED chip. Proceedings, ISTFA 2006: Discretes, Passives, MEMS, and Optoelectronics, pp. 137–141, 2006.

Saraswat K, Kapur P, Souri S. Performance limitations of metal interconnects and possible alternatives. 203<sup>rd</sup> Meeting of the Electrochemical Society, Paris, France, April 2003.

Saraswat K, Kapur P, Chandra G, Chiang T-Y, Souri S. Scaling induced performance limitations of metal interconnects. IEEE ISSCC Microprocessor Design Workshop, San Francisco, CA, February 2002.

Chiang T, Souri S, Chui C, Saraswat K. Thermal analysis of heterogeneous 3-D ICs with various integration scenarios. IEEE IEDM, December 2001.

Banerjee K, Souri S, Kapur P, Saraswat K. 3-D Heterogeneous ICs: A technology for the next decade and beyond. 5<sup>th</sup> IEEE Workshop on Signal Propagation on Interconnects, Venice, Italy, May 2001.

Banerjee K, Souri S, Kapur P, Saraswat K. 3-D ICs: A novel chip design for improving deep-submicrometer interconnect performance and systems-on-chip integration. Proceedings, IEEE: Special Issue on Interconnections, Vol. 89, No. 5, pp. 602–633, May 2001.

Davis J, Venkatesan R, Kaloyeros A, Bylansky M, Souri S, Banerjee K, Saraswat K, Rahman A, Reif R, Meindl J. Integration limits on Gigascale Integration (GSI) in the 21<sup>st</sup> Century. Proceedings, IEEE: Special Issue of Limits to Semiconductor Technology, Vol. 89, No. 3, pp. 3-05–324, March 2001.

Saraswat K, Banerjee K, Joshi A, Kalvade P, Kapur P, Souri S. 3-D ICs: Motivation, performance analysis and technology. Proceedings, 26<sup>th</sup> European Solid-State Circuits Conference (ESSCIRC), Stockholm, Sweden, September 19–21, 2000.

Souri S, Banerjee K, Mehrotra A, Saraswat KC. Multiple Si layer ICs: Motivation, performance analysis, and design implications. 37<sup>th</sup> ACM Design Automation Conference (DAC), pp. 213–220, Los Angeles, CA, June 5–9, 2000.

Saraswat K, Banerjee K, Joshi A, Kalavade P, Souri S, Subramanian V. 3-D ICs with multiple Si Layers: Performance analysis, and technology. 5<sup>th</sup> International Symposium on Low and High Dielectric Constant Materials: Materials Science, Processing, and Reliability Issues, 197<sup>th</sup> Meeting of the Electrochemical Society, Toronto, Canada, May 14–19, 2000.

Saraswat K, Souri S, Subramanian V, Joshi A, Wang A. Novel 3-D structures. Proceedings, IEEE International SOI Conference, pp. 54–55, 1999.

Subramanian V, Toita M, Ibrahim N, Souri S, Saraswat K. Low-leakage germanium-seeded laterally-crystallized single-grain 100nm TFTs for vertical integration applications. IEEE Electron Device Letters, Vol. 20, pp. 341–343, 1999.

Souri S, Saraswat K. Interconnect performance modeling for 3D integrated circuits with multiple Si layers. IEEE International Interconnect Technology Conference, pp. 24–26, 1999.

Haskell B, Souri S, Helfand M. Varistor behavior at twin boundaries in ZnO. Journal of the American Ceramic Society, Vol. 82, No. 8, August 1999.

Chu A, Souri S, Melfand M, Kinsman K, Dupon R. Superior electrical performance of Raychem ZnO Varistor through advanced processing. Proceedings, 1<sup>st</sup> Asian Meeting on Ferroelectricity, Xian, China, October 5–8, 1995.

### **Book Chapters**

Souri S, Chiang T, Kapur P, Banerjee K, Saraswat KC. 3-D ICs deep submicron interconnect performance modeling and analysis. In: Interconnect Technology and Design for Gigascale Integration. Davis J and Meindl J (eds), Kluwer Academic Publishers, October 2003.

### **Speaker Engagements**

Souri S. 3-Dimensional ICs interconnect architecture, technology and performance analysis. Oral Defense, Stanford University, 2003.

Souri S. 3-D ICs with multiple Si Layers: performance analysis and technology. Solid State Technology and Devices Seminar, Microlab, UC Berkeley, 2001.

Souri S. 3D ICs: Performance, analysis and technology. Integrated Circuits and Technology Seminar, Stanford University, 2001.

Souri S. Photorefectance microscopy of semiconductor materials. Raychem Corporation, CR&D, Menlo Park, CA, 1994.

#### **Prior Experience**

Founder, Merenga Inc., 2000–2002

Co-Founder and Engineering Manager, arcadiaOne, Inc., 1999–2000

Research Engineer, Circuit Protection Division, Raychem, 1996–1997

Research Scientist, Corporate Research & Development, Raychem, 1994–1996

#### **Professional Affiliations**

- Institute of Electrical and Electronic Engineers (senior member)
- Oxford University Society (life member)
- Oxford Union (member)